Claims

[c1] What is claimed is:

1.An integrated circuit, comprising:

a plurality of separate memory arrays each having a respective one of a plurality of inputs and a respective one of a plurality of outputs, each output providing an output value indicative of whether a storage location associated with an applied address is passing or failing; and

a shared built-in self-test (BIST) and repair system, coupled to all of the plurality of inputs and all of the plurality of outputs, that applies addresses and data to the plurality of inputs to test the plurality of memory arrays for failing storage locations and, responsive to detection of a failing storage location in any of the plurality of memory arrays, applies a common address remapping to all of the plurality of memory arrays to remap, in each memory array, the address associated with the failing storage location to a different storage location.

[c2] 2.The integrated circuit of Claim 1, wherein the shared BIST and repair system includes:

a pattern generator that generates data patterns to be applied to said plurality of memory arrays;

combination logic, coupled to all of said plurality of outputs, that aggregates addresses indicated as associated with failing storage locations by said output values to obtain a composite listing of failing addresses representing all failing addresses in all of said plurality of memory arrays; and

non-volatile storage, coupled to said plurality of memory arrays, that

res a common remapping for each failing address in said composite listing of failing addresses and that supplies each common remapping to all of said plurality of memory arrays.

[c3] 3.The integrated circuit of Claim 2, wherein:
each of said plurality of outputs provides an output value that is an individual failure indication; and
said combination logic includes an OR gate that combines said plurality of outputs to produce single combined failure indication for an applied address for all of said plurality of memory arrays.

[c4] 4.The integrated circuit of Claim 2, wherein said non-volatile storage comprises a plurality of laser-programmable fuses.

[c5] 5.The integrated circuit of Claim 2, wherein said non-volatile storage comprises electrically programmable storage.

[c6] 6.The integrated circuit of Claim 2, wherein said non-volatile storage stores said common remapping of each failing address in compressed format.

[c7] 7.The integrated circuit of Claim 6, wherein:
said shared BIST and repair system is a first BIST and repair system;
said electrically programmable storage stores at least one address remapping for another memory array having a second BIST and repair system associated therewith; and
one of said plurality of memory arrays includes a test output port coupled to said another memory array to communicate said at least one address

remapping to said another memory array.

[c8] 8.The integrated circuit of Claim 2, wherein said plurality of memory arrays comprises a plurality of volatile memory arrays, wherein each of said plurality of volatile memory arrays includes repair register file (RRF), coupled to said non-volatile storage, for storing each common remapping supplied by said non-volatile storage.

[c9] 9.The integrated circuit of Claim 1, wherein the storage location that, prior to remapping, was originally associated with the address in at least one of said plurality of memory arrays is a passing storage location.

[c10] 10.The integrated circuit of Claim 1, wherein said integrated circuit comprises a processor chip including data processing functional logic coupled to said plurality of memory arrays.

[c11] 11.A data processing system, including:
a plurality of integrated circuit chips, including at least one processor chip in accordance with Claim 10; and
an interconnect network coupling said plurality of integrated circuit chips.

[c12] 12.A method of detecting and providing a repair for a defect in an integrated circuit including a plurality of separate memory arrays, said method comprising:
testing each of the plurality of memory arrays to detect whether a storage location associated with an applied address is passing or failing; and
in response to detection of a failing storage location in any of the plurality of memory arrays, said failing storage location being associated with a

articular address, storing in non-volatile storage a common address remapping for all of the plurality of memory arrays, wherein said common address remapping indicates a remapping, in each memory array, of the particular address associated with the failing storage location to a different storage location.

[c13] 13.The method of Claim 12, wherein:
said testing further comprises:
generating data patterns to be applied to said plurality of memory arrays utilizing a shared pattern generator;
aggregating addresses indicated as associated with failing storage locations to obtain a composite listing of failing addresses representing all failing addresses in all of said plurality of memory arrays; and
wherein said composite listing is stored in said non-volatile storage.

[c14] 14.The method of Claim 12, wherein said storing comprises storing said common remapping for each failing address utilizing a plurality of laser-programmable fuses.

[c15] 15.The method of Claim 12, wherein said storing comprises storing said common remapping for each failing address utilizing electrically programmable storage.

[c16] 16.The method of Claim 12, wherein said storing comprises storing said common remapping of each failing address in compressed format.

[c17] 17.The method of Claim 16, wherein
said non-volatile storage stores at least one address remapping for

another memory array not belonging to said plurality of memory arrays; and

said method further comprises forwarding said at least one address remapping from one of said plurality of memory arrays to said another memory array.

[c18] 18.The method of Claim 12, wherein said plurality of memory arrays comprises a plurality of volatile memory arrays, said method further comprising:

each of said plurality of volatile memory arrays storing each common remapping in respective repair register file (RRF).

[c19] 19.The method of Claim 12, wherein, in at least one of said plurality of memory arrays, the storage location that, prior to remapping, was associated with the particular address is a passing storage location.

[c20] 20.A method of representing an integrated circuit design, said method comprising:

in one or more first design language statements, defining a plurality of separate memory arrays each having a respective one of a plurality of inputs and a respective one of a plurality of outputs, each output providing an output value indicative of whether a storage location associated with an applied address is passing or failing;

in one or more second design language statement, defining a shared built-in self-test (BIST) and repair system, coupled to all of the plurality of inputs and all of the plurality of outputs, that applies addresses and data to the plurality of inputs to test the plurality of memory arrays for failing

storage locations and, responsive to detection of a failing storage location in any of the plurality of memory arrays, applies a common address remapping to all of the plurality of memory arrays to remap, in each memory array, the address associated with the failing storage location to a different storage location; and

storing said one or more first design language statements and said one or more second design language statements in one or more design files.

[c21] 21.A program product, comprising:

a computer usable medium;

an integrated circuit design within said computer usable medium, said integrated circuit design including:

one or more first design language statements defining a plurality of separate memory arrays each having a respective one of a plurality of inputs and a respective one of a plurality of outputs, each output providing an output value indicative of whether a storage location associated with an applied address is passing or failing; and

one or more second design language statements defining a shared built-in self-test (BIST) and repair system, coupled to all of the plurality of inputs and all of the plurality of outputs, that applies addresses and data to the plurality of inputs to test the plurality of memory arrays for failing storage locations and, responsive to detection of a failing storage location in any of the plurality of memory arrays, applies a common address remapping to all of the plurality of memory arrays to remap, in each memory array, the address associated with the failing storage location to a different storage location.